Scott Nidell

Lab 9 Notes

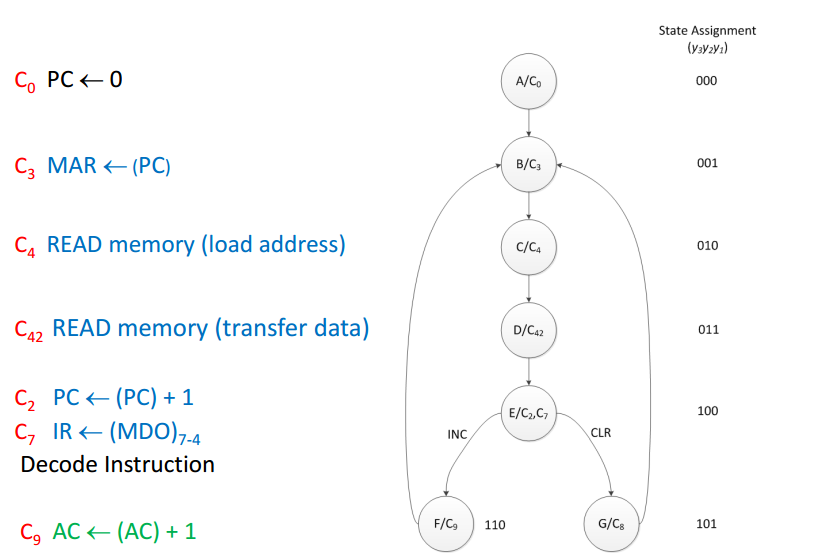
1000921465

CSE 2441-001

**Introduction:** Lab 9 realizes a controller for the CSE 2441 final project. This controller is to capture the first two instruction sets: Clear Accumulator and Increment Accumulator. As discussed in class these instructions share the same fetch and decode steps and will use this knowledge to provide a more efficient state diagram.

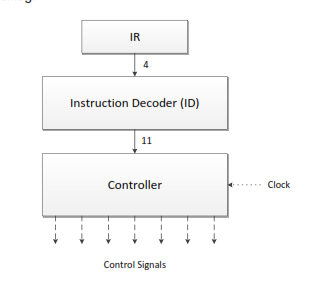
**Theory:**  Using the slides from class we create the basis of the controller from the state diagram in the slides (Figure 1).

**Figure 1:** *State diagram for TRISC controller*



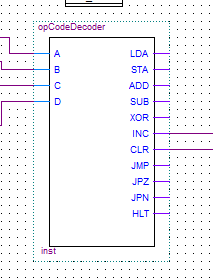
Using this diagram we can break down the control signals in each state. Multiple choices for this lab have been presented. A traditional FSM using hardware, a Phase based design using hardware and a binary controller and Verilog. It was chosen that this lab be completed in Verilog. This Lab also has two parts the Instruction Decoder and the controller (Figure 2).

**Figure 2:** *Lab structure overview*

**

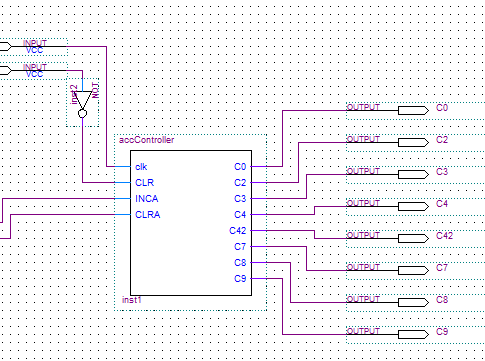
The Instruction Decoder was also constructed in Verilog (Figure 3). This unit is to take a binary opcode and provide a single control signal to the TRISC controller. The controller will use this signal to make branching decisions in the state diagram.

**Figure 3:** *Instruction Decoder*

**

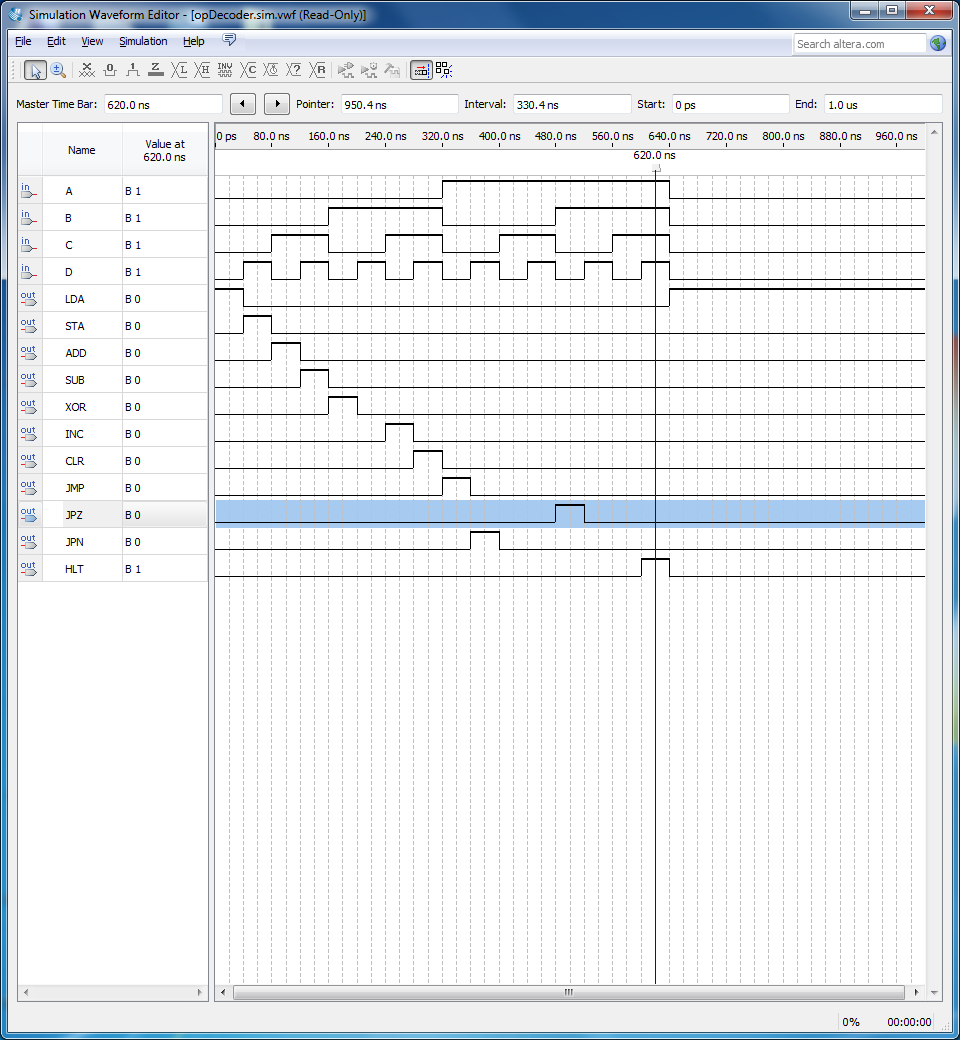
The next phase of Lab 9 is the TRISC controller itself (Figure 4). This will provide control signals to the Program Counter, Memory Address Register, Accumulator, ALU, Memory, and Instruction Register in the final project. This lab however will only control the Accumulator.

**Figure 4:** *TRISC Controller for Lab 9*

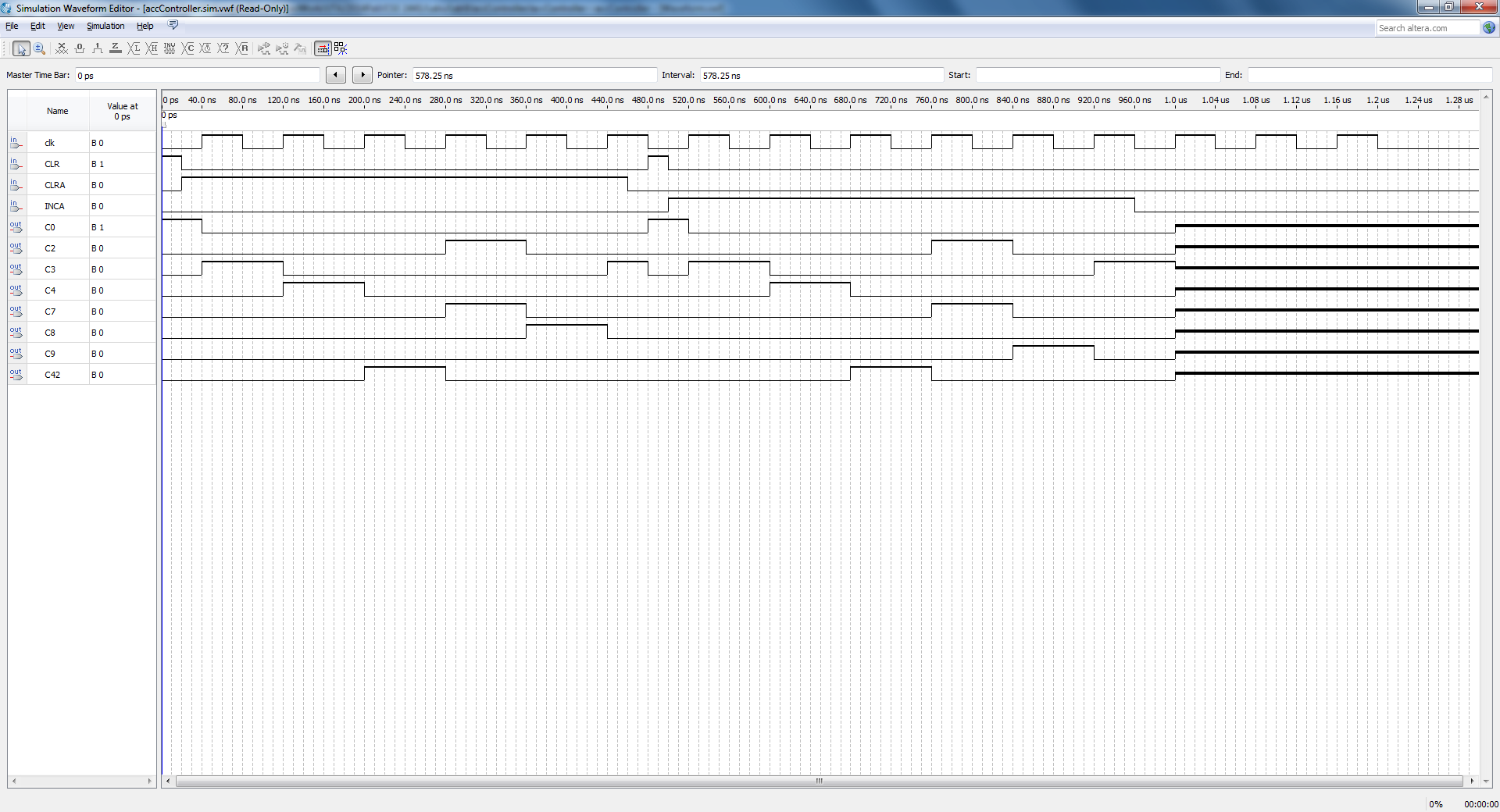


Now that all the units are completed they need to be integrated and tested. These modules were both unit tested and integration tested (Figure 5, 6, 7).

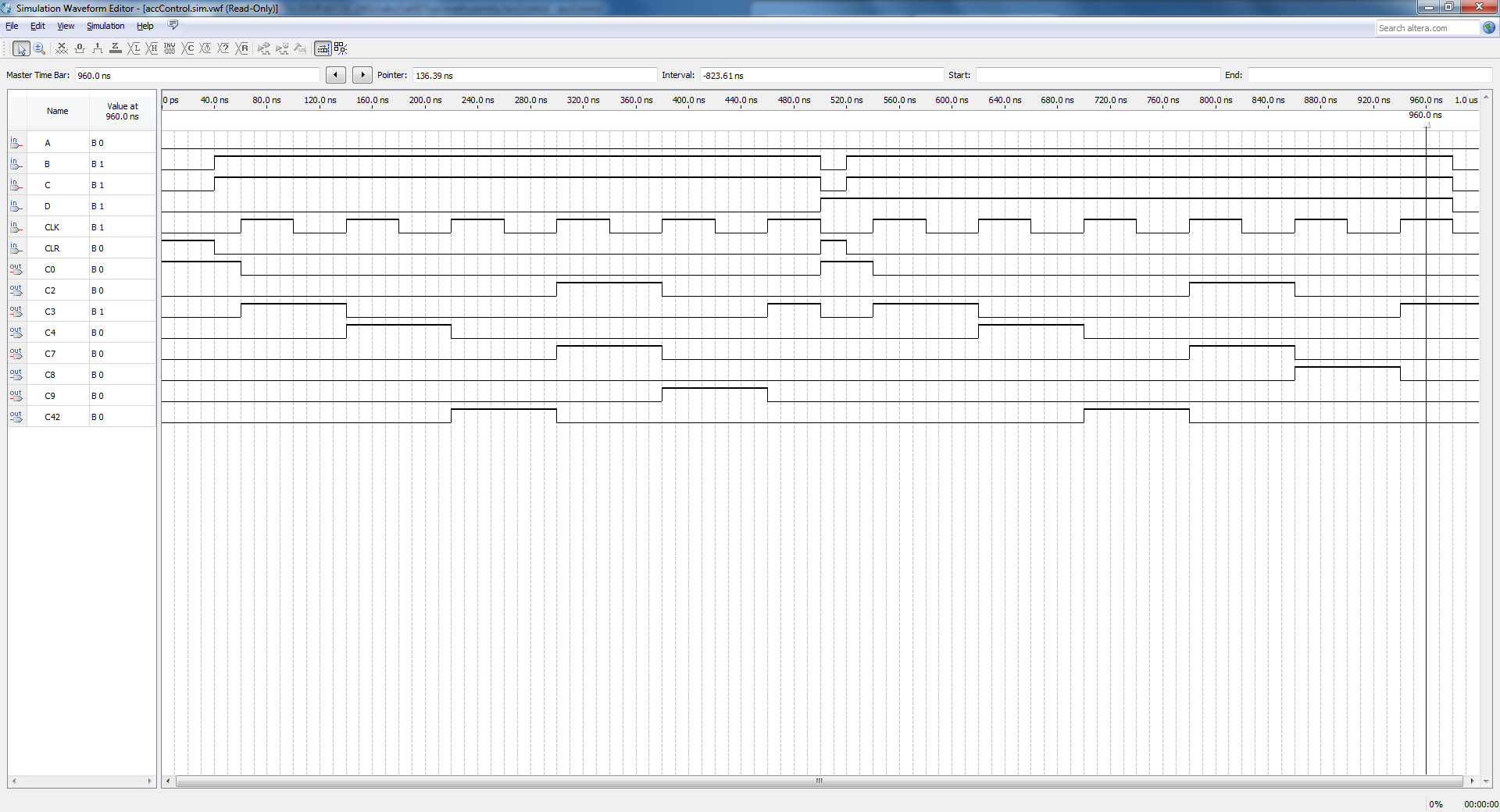
**Figure 5:** *Waveform for opcode decoder.*



**Figure 6:** *Waveform for Lab 9TRISC controller*

**

**Figure 7:** *Waveform for integrated controller and opcode decoder*

**

Once the testing has been completed pin assignments were created and the design was programmed onto the DE1 for demonstration. Using multiple LED’s for C0, C2 ,C3 ,C4 ,C42 ,C8 and C9 and also Key 1 and Key0 for the clock and control Clear. Lab time is then used for demonstration

**Conclusion:** This lab came with some increased troubleshooting. Using Verilog to create a state machine this size is new ground for our design. Using the case statements along with timing, and multiple if/if else/else statements to create the correct control response was difficult. However, this I believe will be easier to transition Lab9 into a fully realized controller for the final project.